Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **1Y**
2. **1A**
3. **1B**
4. **2Y**
5. **2A**
6. **2B**
7. **GND**
8. **3A**
9. **3B**
10. **3Y**
11. **4A**
12. **4B**
13. **4Y**
14. **VCC**

**.047”**

**8**

**7**

**6**

**12 11 10 9**

**2 3 4 5**

**13**

**14**

**1**

**ACT02**

**MASK**

**REF**

**.055”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004 X .004”**

**Backside Potential:**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .047” X .055” DATE: 3/14/23**

**MFG: SILICON SUPPLIES THICKNESS .014” P/N: 54ACT02**

**DG 10.1.2**

#### Rev B, 7/1